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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/484,549

01/18/2000

Korbin Van Dyke

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05/15/2006

ATI TECHNOLOGIES, INC.

C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.

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CHICAGO, IL 60601

EXAMINER

VO, LILIAN

ART UNIT

PAPER NUMBER

2195

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

E

**Office Action Summary**

Application No.

09/484,549

Applicant(s)

DYKE ET AL.

Examiner

Lilian Vo

Art Unit

2195

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 February 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2 - 12 and 15 - 17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2 - 12 and 15 - 17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. Claims 2-12 and 15- 17 are presented for examination. Claims 1, 13 and 14 have been cancelled.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/23/2006 has been entered.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:  
  
The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
4. Claim 17 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As to **claim 17**, there is a lack of written description in the specification which specifically states that the allocating of the program code among the plurality of processors for processing is done without regard to a processor mode.

Appropriate correction is required to overcome this type of rejection.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 2 – 12 and 15 – 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Bonola (USPN 5,706,514).

7. As per **claim 15**, Bonola teaches the invention as claimed, including a method for providing multimedia functionality in a homogeneous multiprocessor environment comprising:

queuing tasks (col. 3 lines 61-65);

identifying available processing resources in the homogeneous multiprocessor environment (col. 7 lines 36-38);

allocating the available processing resources among the tasks based on the capabilities of each of the available processing resources and the processing requirements of each of the tasks (col. 7 lines 42-52; col. 8 lines 11-13);

providing to the available processing resources functional programs and initial data corresponding to the tasks (col. 8, lines 13 – 18); and

performing the tasks using the available processing resources to produce resulting data (col. 9 lines 13-23), wherein the functional programs cause the available processing resources to perform the tasks of at least one of: graphics image processing, video processing, audio processing and communications processing (col. 1 lines 15-26, wherein graphic image processing, video processing, audio processing, and communication processing are just some of the types of tasks that can be performed on an x86 system).

8. As per **claim 2**, Bonola teaches the invention as claimed, including the method of claim 15 wherein a plurality of processors of the homogeneous multiprocessor environment are capable of executing a first instruction of a first instruction set and a second instruction of a second instruction set (col. 2 lines 6-10; col. 3 lines 37-44).

9. As per **claim 3**, Bonola teaches the invention as claimed, including the method of claim 2 wherein the first instruction and the second instruction share an identical bit pattern but perform different operations (col. 1 lines 15-26).

10. As per **claim 4**, Bonola teaches the invention as claimed, including the method of claim 3 wherein a first processor of the plurality of processors executes an input/output kernel program, the input/output kernel program including a first portion expressed using the first instruction set and a second portion expressed using the second instruction set (col. 3 lines 26-35; col. 7 lines 22-33).

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11. As per **claim 5**, Bonola teaches the invention as claimed, including the method of claim 3 further comprising the step of:

converting a functional program of the functional programs expressed using the first instruction set to an equivalent functional program expressed using the second instruction set (col. 8 lines 31-45).

12. As per **claim 6**, Bonola teaches the invention as claimed, including the method of claim 3 wherein the tasks comprise x86 processing (col. 1 lines 15-26, wherein graphic image processing, video processing, audio processing, and communication processing are just some of the types of tasks that can be performed on an x86 system).

13. As per **claim 7**, Bonola teaches the invention as claimed, including the method of claim 3 further comprising the step of:

receiving the initial data from a first input/output device (col. 8 lines 11-15).

14. As per **claim 8**, Bonola teaches the invention as claimed, including the method of claim 3 further comprising the step of:

passing the resulting data to a first input/output device (col. 9 lines 13-23).

15. As per **claim 9**, Bonola teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to the first input/output device further comprises the step of:

passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device (col. 9 lines 13-23).

16. As per **claim 10**, Bonola teaches the invention as claimed, including the method of claim 9 wherein the step of passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device further comprises the step of:

automatically adapting to a reallocation of the available processing resources among the tasks (col. 8 lines 46-65).

17. As per **claim 11**, Bonola teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to a first input/output device further comprises the step of:

passing the resulting data to a mixed-signal device (col. 9 13-15, 19-23).

18. As per **claim 12**, Bonola teaches the invention as claimed, including the method of claim 3 wherein the step of allocating the available processing resources among the tasks is dynamically adjusted (col. 8 lines 46-65).

19. As per **claim 16**, Bonola teaches the invention as claimed, including the method of claim 15, further comprising:

keeping track, remotely from the resources, of the capabilities of all available processing resources (col. 7 lines 42-52); and

identifying available processing resources in the homogeneous multiprocessor environment based solely on the capabilities kept track of remotely (col. 7 lines 36-38, 42-52).

### *Claim Rejections - 35 USC § 103*

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

21. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bonola (USPN 5,706,514).

22. As per **claim 17**, Bonola teaches the invention as claimed, including an apparatus comprising:

a plurality of processors coupled to a bus (col. 4 lines 29-33; Fig. 1);

an input/output interface coupled to the bus (col. 4 lines 52-54; Fig. 1);

a plurality of input/output devices coupled to the input/output interface (col. 4 lines 52 - 57, Fig. 1), the plurality of processors processing program code configured to perform a plurality of tasks (col. 9 lines 24-27), the program code comprising:

program code configured to cause a first portion of the plurality of processors to interact with a first input/output device of the plurality of input/output devices (col. 7 lines 22-25);



program code configured to cause a second portion of the plurality of processors to interact with a second input/output device of the plurality of input/output devices (col. 7 lines 42 - 52);

program code configured to cause a second portion of the plurality of processors to emulate a specific microprocessor instruction set (col. 8 lines 11-18);

wherein the first portion of the plurality of processors provides functionality as found in a first application-specific subsystem and wherein the first input/output device is the first application-specific subsystem (col. 3 lines 23-30); and

wherein the second portion of the plurality of processors provides functionality as found in a second application-specific subsystem and wherein the second input/output device is the second application-specific subsystem (col. 7 lines 42-52; col. 8 lines 11-18); and

kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors without regard to a processor mode (col. 3 lines 26-35; col. 7 lines 22-33; col. 8 lines 11 -18).

With respect to the limitation of kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors without regard to a processor mode, Bonola discloses “a technique for handling processor mode mismatched instructions or commands encountered by a CPU within multiprocessor computer system...if a multimode processor encounters a command or instruction that it cannot execute without shifting modes or mode emulation, it will look for an alternate processor present in the computer system to instead handle the mode mismatched command...” In other words, Bonola’s system can perform the resource allocation among the processors regardless of a processor mode. Thus, the

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limitation narrowed by the claim is considered obvious over Bonola since applicant has not disclosed that limitation solves any stated problem or is for any particular purpose and it appears that Bonola's system is capable of perform the functions as claimed equally well. Therefore, it would have been obvious to one of an ordinary skill in the art, at the time the invention was made to utilize the features as disclosed by Bonola to perform the tasks as desired.

### *Response to Arguments*

23. Applicant's arguments with respect to claim 17 have been considered but are moot in view of the new ground(s) of rejection.

24. Applicant argues that the claims are distinct from Bonola based on the limitations in the independent claims directed to performance of "graphics image processing, video processing and audio processing and communications processing." However, these features are merely a recitation of the intended use of the claimed invention. Such an intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. By loading a processor with the information necessary to proceed with processing of a particular task, the processors may perform any of graphics image processing, video processing, audio processing, or communications processing.

With respect to applicant's remarks regarding MPEP 2112.02 stating that "the discovery of a new use for an old structure based on unknown properties of the structure might be

patentable to the discoverer as a process of using". MPEP 2112 also states that "the claiming of a new use, new function or unknown property which is inherently present in the prior does not necessarily make the claim patentable... Under the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed will be considered described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. *In re King*, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986)".

Therefore, applicant is directed to col. 3 lines 26 – 35 and fig. 1 in which Bonola discloses the processors execute an input/output kernel program and the processors communicate with input output devices 62, 68, 71, etc. One of an ordinary skill in the art would recognize that based on such disclosure, at least the communication processing task is inherently being performed by the processor.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Thursday 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

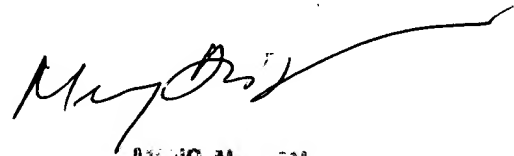
Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist at 571-272-2100.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo  
Examiner  
Art Unit 2195

lv  
May 6, 2006



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